CLAIMS

What is claimed is:

1. A data detector, comprising:

a delay logic, receiving an unfiltered input signal in quadrature and in-phase components, and applying a delay to each of the in-phase and quadrature phase components of the unfiltered input signal;

a first multiplication logic, the first multiplication logic multiplying the delayed in-phase component of the unfiltered input signal by the quadrature phase component of the unfiltered input signal to obtain a first multiplication result;

a second multiplication logic, the second multiplication logic multiplying the delayed quadrature phase component of the unfiltered input signal by the in-phase component of the unfiltered input signal to obtain a second multiplication result; and

an adder, the adder adding the first multiplication result with the second multiplication result and generating a decision signal.

2. The data detector as defined in claim 1, wherein the delay logic comprises at least one shift registers.

3. The data detector as defined in claim 2, wherein the delay applied by the delay logic is approximately equal to a symbol period.

4. The data detector as defined in claim 3, wherein the delay logic has a sampling rate of about 50 million samples per second.

5. The data detector as defined in claim 2, wherein the delay period of the delay logic is adjustable, allowing for frequency offset compensation.

6. The data detector as defined in claim 5, wherein the delay logic comprises a multi-stage delay.

7. The data detector as defined in claim 1, wherein the data detector further comprises a post-detection correction logic, the post-detection correction logic being applied to the decision signal and reducing inter-symbol interference.

8. The data detector as defined in claim 7, wherein the post-detection correction comprises:

a test logic, the test logic receiving the decision signal and asserting a selection signal when the absolute value of the decision signal exceeds a threshold; and

a multiplexer, receiving the selection signal, the decision signal and an inversion of a previously corrected signal, the selection signal being used to decide whether to output the decision signal or the inversion of a previously corrected signal, and producing a post-detection corrected signal.

9. A data detector, comprising:

a delay logic, receiving an input signal in quadrature and in-phase components, and applying a delay to each of the in-phase and quadrature phase

components of the input signal, wherein the delay is adjustable, allowing for frequency offset compensation;

a first multiplication logic, the first multiplication logic multiplying the delayed in-phase component of the input signal by the quadrature phase component of the input signal to obtain a first multiplication result;

a second multiplication logic, the second multiplication logic multiplying the delayed quadrature phase component of the input signal being by the in-phase component of the input signal to obtain a second multiplication result; and

an adder, the adder adding the first multiplication result with the second multiplication result generating a decision signal.

10. The data detector as defined in claim 9, wherein the delay logic comprises at least one shift register, and the delay applied by the delay logic is approximately equal to a symbol period.

11. The data detector as defined in claim 10, wherein the delay logic has a sampling rate of about 50 million samples per second.

12. The data detector as defined in claim 10, wherein the delay logic comprises a multi-stage delay.

13. The data detector as defined in claim 9, wherein the data detector further comprises a post-detection correction logic, the post-detection correction logic being applied to the decision signal and reducing inter-symbol interference.

14. The data detector as defined in claim 13, wherein the post-detection correction comprises:

a test logic, the test logic receiving the decision signal and asserting a selection signal when the absolute value of the decision signal exceeds a threshold; and

a multiplexer, receiving the selection signal, the decision signal and an inversion of a previously corrected signal, the selection signal being used to decide whether to output the decision signal or the inversion of a previously corrected signal, and producing a post-detection corrected signal.

15. A method for detecting data, the method comprising the steps of:

receiving an unfiltered input signal having an in-phase component and a quadrature phase component;

delaying the in-phase and quadrature phase components of the input signal;

multiplying the in-phase component of the input signal by the delayed quadrature phase component of the input signal to yield a first result;

multiplying the delayed in-phase component of the input signal by the quadrature phase component of the input signal to yield a second result; and

summing the first and second results to obtain a decision signal.

16. The method as defined in claim 15, wherein the method further comprises a post-detection correction method comprising the steps of:

testing to find whether the absolute value of the decision variable exceeds a threshold;

sending the result of the test to the selection input of a multiplexer; and

outputting the decision variable from the multiplexer if it exceeds a certain threshold, otherwise choosing an inversion of the previous multiplexer output.

17. The method as defined in claim 15, wherein delaying of the in-phase and quadrature phase signals is approximately equal to a symbol period.

18. The method as defined in claim 17, wherein the delay is realized using shift registers which sample at the rate of about 50 million samples per second.

19. The method as defined in claim 15, wherein the method further comprises adjusting the delay, to allow for frequency offset compensation.

20. The method as defined in claim 19, wherein the adjustment occurs during a transmission preamble, and comprises a two stage adjustment, the first being a rough compensation at the beginning of the preamble and the second being a fine compensation at the end of the preamble.

21. A method for detecting data, the method comprising the steps of:

receiving an input signal having an in-phase component and a quadrature phase component;

delaying the in-phase and quadrature phase components of the input signal;

multiplying the in-phase component of the input signal by the delayed quadrature phase component of the input signal to yield a first result;

multiplying the delayed in-phase component of the input signal by the quadrature phase component of the input signal to yield a second result;

summing the first and second results to obtain a decision signal; and

compensating for a frequency offset.

22. The method as defined in claim 21, wherein the method further comprises a post-detection correction method comprising the steps of:

testing to find whether the absolute value of the decision variable exceeds a threshold;

sending the result of the test to the selection input of a multiplexer; and

outputting the decision variable from the multiplexer if it exceeds a certain threshold, otherwise choosing an inversion of the previous multiplexer output.

23. The method as defined in claim 21, wherein the delay of the in-phase and quadrature phase components is approximately equal to a symbol period.

24. The method as defined in claim 23, wherein the delay is realized using shift registers which sample at the rate of about 50 million samples per second.

25. The method as defined in claim 21, wherein the frequency offset compensation comprises adjusting the delay.

26. The method as defined in claim 25, wherein the adjustment occurs during a transmission preamble, and comprises a two stage adjustment, the first being a rough compensation at the beginning of the preamble and the second being a fine compensation at the end of the preamble.

27. A data detection system comprising:

means for receiving an unfiltered input signal comprising an in-phase component and a quadrature phase component;

means for delaying the in-phase and quadrature phase components;

means for first multiplication, multiplying the in-phase component by the delayed quadrature phase component;

means for second multiplication, multiplying the delayed in-phase component by the quadrature phase component; and

means for summing the result of the first multiplication with the result of the second multiplication to receive a decision variable.

28. The system as defined in claim 27, wherein the data detector further comprises a post detection correction means.

29. The system as defined in claim 28, wherein the post detection correction means comprises:

means for testing whether the absolute value of the decision variable exceeds a threshold; and

means for outputting either the decision variable or an inversion of the previous output, depending on the result of the testing means.

30. The data detector as defined in claim 27, wherein the delay means delay the signal by approximately one symbol period.

31. The data detector as defined in claim 30, wherein the delay means are shift registers which sample at a rate of about 50 million samples per second.

32. The data detector as defined in claim 27, wherein the data detection further comprises a means for compensating for frequency offset.

33. The data detector as defined in claim 32, wherein the frequency offset compensation means comprises making the delay means adjustable.

34. The data detector as defined in claim 33, wherein the adjustable delay means comprise both a rough compensation at a the beginning of a preamble transmission and a fine compensation at the end of the preamble transmission.

35. A radio receiver chain, comprising:

an antenna capable of receiving a radio signal;

an input band selection filter coupled to the antenna;

a low noise amplifier, coupled to the output of the input band selection filter;

a first mixer for deriving an in-phase signal, coupled to the output of the low noise amplifier;

a second mixer for deriving a quadrature phase signal, coupled to the output of the low noise amplifier;

a channel selection filter, coupled to the in-phase and quadrature phase signals;

a first limiting amplifier, coupled to the in-phase output of the channel selection filter and capable of sampling the in-phase signal;

a second limiting amplifier, coupled to the quadrature phase output of the channel selection filter and capable of sampling the quadrature phase signal;

a data detector comprising:

an in-phase and a quadrature phase signal, without any finite impulse response filtering;

a first delay element, delaying the in-phase signal;

a second delay element, delaying the quadrature phase signal;

a first multiplier, multiplying the in-phase signal by the delayed quadrature phase signal;

a second multiplier, multiplying the quadrature phase signal by the delayed in-phase signal; and

an adder, summing the result of the first and second multipliers to derive a decision signal.

36. The radio receiver chain as defined in claim 35, wherein the chain further comprises a post detection filter receiving the decision variable and removing odd order cross components.

37. The radio receiver chain as defined in claim 36, wherein the chain further comprises a post detection correction algorithm, comprising a multiplexer having two inputs and a selection signal, the first input comprising the output of the post detection filter, the second input comprising a delayed inversion of the previous multiplexer output, and the selection signal comprising a test result, wherein the test is whether the absolute value of the output of the post detection filter is greater than a threshold value.

38. The radio receiver chain as defined in claim 22, wherein the delay is chosen such that it is approximately one symbol period.

39. The radio receiver chain as defined in claim 22, wherein the delay is comprised of a plurality of shift registers, and the chain further comprises a delay selection to adjust the delay according to which delay fits the incoming frequency to most effectively detect the data.